

## FEATURES

**44 V supply maximum ratings**

**V<sub>SS</sub> to V<sub>DD</sub> analog signal range**

**Low on resistance (<70 Ω)**

**Low ΔR<sub>ON</sub> (9 Ω max)**

**Low R<sub>ON</sub> match (3 Ω max)**

**Low power dissipation**

**Fast switching times**

**t<sub>ON</sub> < 110 ns**

**t<sub>OFF</sub> < 60 ns**

**Low leakage currents (3 nA max)**

**Low charge injection (6 pC max)**

**Break-before-make switching action**

**Latch-up proof A grade**

**Plug-in upgrade for DG201A/ADG201A, DG202A/ADG202A,  
DG211/ADG211A**

**Plug-in replacement for DG441/DG442/DG444**

## APPLICATIONS

**Audio and video switching**

**Automatic test equipment**

**Precision data acquisition**

**Battery-powered systems**

**Sample-and-hold systems**

**Communication systems**

## GENERAL DESCRIPTION

The [ADG441](#), [ADG442](#), and [ADG444](#) are monolithic CMOS devices that comprise of four independently selectable switches. They are designed on an enhanced LC<sup>2</sup>MOS process that provides low power dissipation yet gives high switching speed and low on resistance.

The on resistance profile is very flat over the full analog input range, which ensures good linearity and low distortion when switching audio signals. High switching speed also makes the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments. The [ADG441](#), [ADG442](#), and [ADG444](#) contain four independent SPST switches. Each switch of the [ADG441](#) and [ADG444](#) turns on when a logic low is applied to the appropriate control input. The [ADG442](#) switches are turned on with logic high on the appropriate control input. The [ADG441](#) and [ADG444](#) switches differ in that the [ADG444](#) requires a 5 V logic power supply that is applied to the V<sub>L</sub> pin. The [ADG441](#) and [ADG442](#) do not have a V<sub>L</sub> pin, the logic power supply is generated internally by an on-chip voltage generator.

## FUNCTIONAL BLOCK DIAGRAM

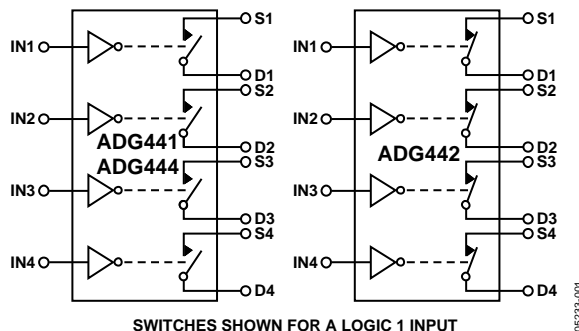


Figure 1.

Each switch conducts equally well in both directions when ON and has an input signal range that extends to the power supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is the low charge injection for minimum transients when switching the digital inputs.

## PRODUCT HIGHLIGHTS

1. Extended signal range. The [ADG441A/ADG442A/ADG444A](#) are fabricated on an enhanced LC<sup>2</sup>MOS, trench-isolated process, giving an increased signal range that extends to the supply rails.
2. Low power dissipation.
3. Low R<sub>ON</sub>.
4. Trench isolation guards against latch-up for A grade parts. A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.
5. Break-before-make switching. This prevents channel shorting when the switches are configured as a multiplexer.
6. Single-supply operation. For applications where the analog signal is unipolar, the [ADG441/ADG442/ADG444](#) can be operated from a single-rail power supply. The parts are fully specified with a single 12 V power supply.

Rev. B

[Document Feedback](#)

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## REVISION HISTORY

### 5/14—Rev. A to Rev. B

Updated Outline Dimensions .....	13
Changes to Ordering Guide .....	14

### 5/05—Rev. 0 to Rev. A

Changes to Format .....	Universal
Deleted CERDIP Package and T Grade .....	Universal
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Updated Outline Dimensions .....	13
Changes to Ordering Guide .....	14

### 4/94—Revision 0: Initial Version

## SPECIFICATIONS

DUAL SUPPLY<sup>1</sup>

$V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $V_L = +5\text{ V} \pm 10\%$  (ADG444), GND = 0 V, unless otherwise noted.

Table 1.

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	−40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		V <sub>SS</sub> to V <sub>DD</sub>	V	
R <sub>ON</sub>	40		Ω typ	V <sub>D</sub> = ±8.5 V, I <sub>S</sub> = −10 mA
	70	85	Ω max	V <sub>DD</sub> = +13.5 V, V <sub>SS</sub> = −13.5 V
ΔR <sub>ON</sub>		4	Ω typ	−8.5 V ≤ V <sub>D</sub> ≤ +8.5 V
		9	Ω max	
R <sub>ON</sub> Match		1	Ω typ	V <sub>D</sub> = 0 V, I <sub>S</sub> = −10 mA
		3	Ω max	
LEAKAGE CURRENTS				
Source OFF Leakage I <sub>S</sub> (OFF)	±0.01		nA typ	V <sub>DD</sub> = +16.5 V, V <sub>SS</sub> = −16.5 V
	±0.5	±3	nA max	V <sub>D</sub> = ±15.5 V, V <sub>S</sub> = ∓15.5 V
Drain OFF Leakage I <sub>D</sub> (OFF)	±0.01		nA typ	See Figure 15
	±0.5	±3	nA max	V <sub>D</sub> = ±15.5 V, V <sub>S</sub> = ∓15.5 V
Channel ON Leakage I <sub>D</sub> , I <sub>S</sub> (ON)	±0.08		nA typ	See Figure 15
	±0.5	±3	nA max	V <sub>S</sub> = V <sub>D</sub> = ±15.5 V
				See Figure 16
DIGITAL INPUTS				
Input High Voltage, V <sub>INH</sub>		2.4	V min	
Input Low Voltage, V <sub>INL</sub>		0.8	V max	
Input Current				
I <sub>INL</sub> or I <sub>INH</sub>		±0.00001	μA typ	V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>
		±0.5	μA max	
DYNAMIC CHARACTERISTICS <sup>2</sup>				
t <sub>ON</sub>	85		ns typ	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 35 pF;
	110	170	ns max	V <sub>S</sub> = ±10 V; see Figure 17
t <sub>OFF</sub>	45		ns typ	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 35 pF;
	60	80	ns max	V <sub>S</sub> = ±10 V; see Figure 17
t <sub>OPEN</sub>	30		ns typ	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 35 pF;
Charge Injection	1		pC typ	V <sub>S</sub> = 0 V, R <sub>S</sub> = 0 Ω, C <sub>L</sub> = 1 nF;
	6		pC max	V <sub>DD</sub> = +15 V, V <sub>SS</sub> = −15 V; see Figure 18
OFF Isolation	60		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF; f = 1 MHz; see Figure 19
Channel-to-Channel Crosstalk	100		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF; f= 1 MHz; see Figure 20
C <sub>S</sub> (OFF)	4		pF typ	f = 1 MHz
C <sub>D</sub> (OFF)	4		pF typ	f = 1 MHz
C <sub>D</sub> , C <sub>S</sub> (ON)	16		pF typ	f = 1 MHz
POWER REQUIREMENTS				
I <sub>DD</sub>				V <sub>DD</sub> = +16.5 V, V <sub>SS</sub> = −16.5 V
		80	μA max	Digital Inputs = 0 V or 5 V
ADG441/ADG442			μA typ	
ADG444	0.001		μA max	
	1	2.5	μA max	
I <sub>SS</sub>	0.0001		μA typ	
	1	2.5	μA max	
I <sub>L</sub> (ADG444 Only)	0.001		μA typ	V <sub>L</sub> = 5.5 V
	1	2.5	μA max	

<sup>1</sup> Temperature range is: B Version: −40°C to +85°C.

<sup>2</sup> Guaranteed by design, not subject to production test.

**SINGLE SUPPLY<sup>1</sup>**

$V_{DD} = +12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $V_L = +5\text{ V} \pm 10\%$  (ADG444), GND = 0 V, unless otherwise noted.

**Table 2.**

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	−40°C to +85°C		
ANALOG SWITCH				
Analog Signal Range		0 to V <sub>DD</sub>	V	
R <sub>ON</sub>	70		Ω typ	V <sub>D</sub> = +3 V, +8 V, I <sub>S</sub> = −5 mA
	110	130	Ω max	V <sub>DD</sub> = 10.8 V
ΔR <sub>ON</sub>		4	Ω typ	3 V ≤ V <sub>D</sub> ≤ 8 V
		9	Ω max	
R <sub>ON</sub> Match		1	Ω typ	V <sub>D</sub> = +6 V, I <sub>S</sub> = −5 mA
		3	Ω max	
LEAKAGE CURRENT				
Source OFF Leakage I <sub>S</sub> (OFF)	±0.01		nA typ	V <sub>DD</sub> = 13.2 V
	±0.5	±3	nA max	V <sub>D</sub> = 12.2 V/1 V, V <sub>S</sub> = 1 V/12.2 V
Drain OFF Leakage I <sub>D</sub> (OFF)	±0.01		nA typ	See Figure 15
	±0.5	±3	nA max	V <sub>D</sub> = 12.2 V/1 V, V <sub>S</sub> = 1 V/12.2 V
Channel ON Leakage I <sub>D</sub> , I <sub>S</sub> (ON)	±0.08		nA typ	See Figure 15
	±0.5	±3	nA max	V <sub>S</sub> = V <sub>D</sub> = 12.2 V/1 V
				Figure 16
DIGITAL INPUTS				
Input High Voltage, V <sub>INH</sub>		2.4	V min	
Input Low Voltage, V <sub>INL</sub>		0.8	V max	
Input Current				
I <sub>INL</sub> or I <sub>INH</sub>		±0.00001	μA typ	V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>
		±0.5	μA max	
DYNAMIC CHARACTERISTICS <sup>2</sup>				
t <sub>ON</sub>	105		ns typ	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 35 pF
	150	220	ns max	V <sub>S</sub> = 8 V; Figure 17
t <sub>OFF</sub>	40		ns typ	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 35 pF
	60	100	ns max	V <sub>S</sub> = 8 V; Figure 17
t <sub>OPEN</sub>	50		ns typ	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 35 pF
Charge Injection	2		pC typ	V <sub>S</sub> = 6 V, R <sub>S</sub> = 0 Ω, C <sub>L</sub> = 1 nF
	6		pC max	V <sub>DD</sub> = 12 V, V <sub>SS</sub> = 0 V; see Figure 18
OFF Isolation	60		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz; see Figure 19
Channel-to-Channel Crosstalk	100		dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz; see Figure 20
C <sub>S</sub> (OFF)	7		pF typ	f = 1 MHz
C <sub>D</sub> (OFF)	10		pF typ	f = 1 MHz
C <sub>D</sub> , C <sub>S</sub> (ON)	16		pF typ	f = 1 MHz
POWER REQUIREMENTS				
I <sub>DD</sub>				V <sub>DD</sub> = 13.2 V
ADG441/ADG442		80	μA max	Digital Inputs = 0 V or 5 V
ADG444	0.001		μA typ	
	1	2.5	μA max	
I <sub>L</sub> (ADG444 Only)	0.001		μA typ	V <sub>L</sub> = 5.5 V
	1	2.5	μA max	

<sup>1</sup> Temperature range is: B Version: –40°C to +85°C.

<sup>2</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$  unless otherwise noted.

**Table 3.**

Parameter	Rating
$V_{DD}$ to $V_{SS}$	44 V
$V_{DD}$ to GND	−0.3 V to +25 V
$V_{SS}$ to GND	+0.3 V to −25 V
$V_L$ to GND	−0.3 V to $V_{DD} + 0.3$ V
Analog, Digital Inputs	$V_{SS} - 2$ V to $V_{DD} + 2$ V or 30 mA, Whichever Occurs First
Continuous Current, S or D	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max)	100 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature, Soldering (10 sec)	300°C
Plastic Package, Power Dissipation	470 mW
$\theta_{JA}$ , Thermal Impedance	177°C/W
Lead Temperature, Soldering (10 sec)	260°C
SOIC Package, Power Dissipation	600 mW
$\theta_{JA}$ , Thermal Impedance	77°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Truth Table**

ADG441/ADG444 IN	ADG442 IN	Switch Condition
0	1	ON
1	0	OFF

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

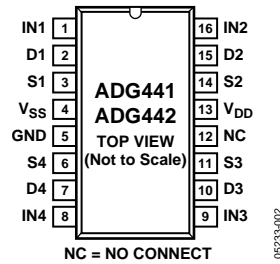


Figure 2. ADG441/ADG442 (DIP/SOIC)

Table 5. ADG441/ADG442 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 9, 16	IN1 to IN4	Logic Control Input.
2, 7, 10, 15	D1 to D4	Drain Terminal. May be an input or output.
3, 6, 11, 14	S1 to S4	Source Terminal. May be an input or output.
4	V <sub>SS</sub>	Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it may be connected to ground.
5	GND	Ground (0 V) Reference.
12	NC	No Connect.
13	V <sub>DD</sub>	Most Positive Power Supply Potential.

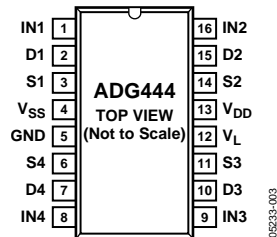


Figure 3. ADG444 (DIP/SOIC)

Table 6. ADG444 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 9, 16	IN1 to IN4	Logic Control Input.
2, 7, 10, 15	D1 to D4	Drain Terminal. May be an input or output.
3, 6, 11, 14	S1 to S4	Source Terminal. May be an input or output.
4	V <sub>SS</sub>	Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it may be connected to ground.
5	GND	Ground (0 V) Reference.
12	V <sub>L</sub>	Logic Power Supply (5 V).
13	V <sub>DD</sub>	Most Positive Power Supply Potential.

## TYPICAL PERFORMANCE CHARACTERISTICS

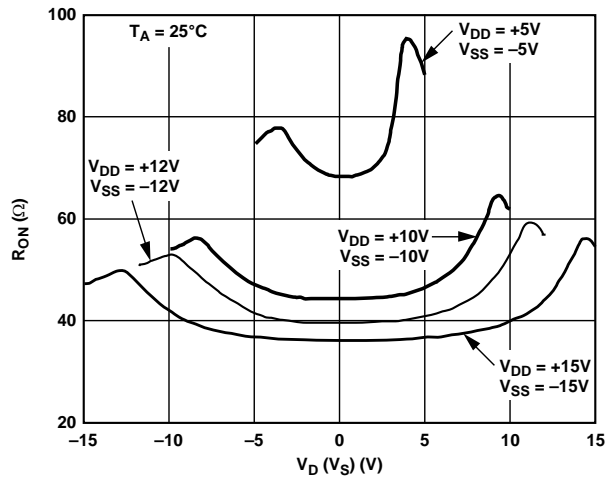
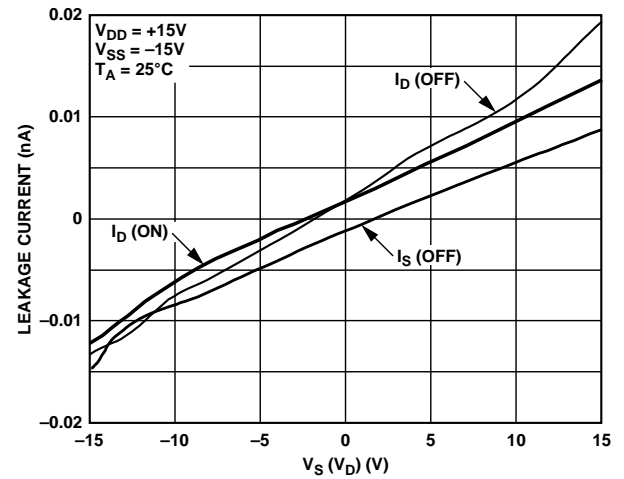
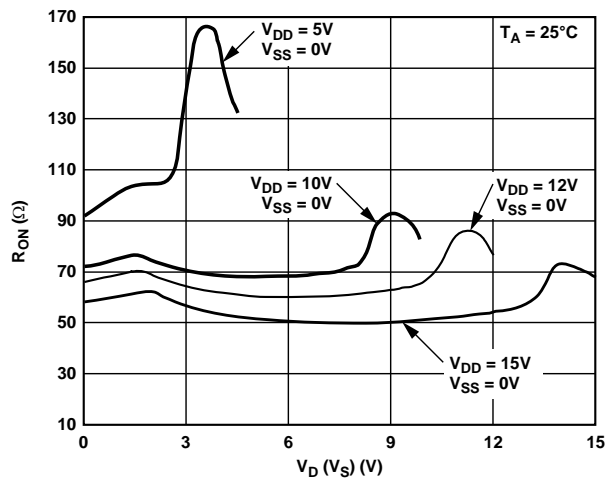
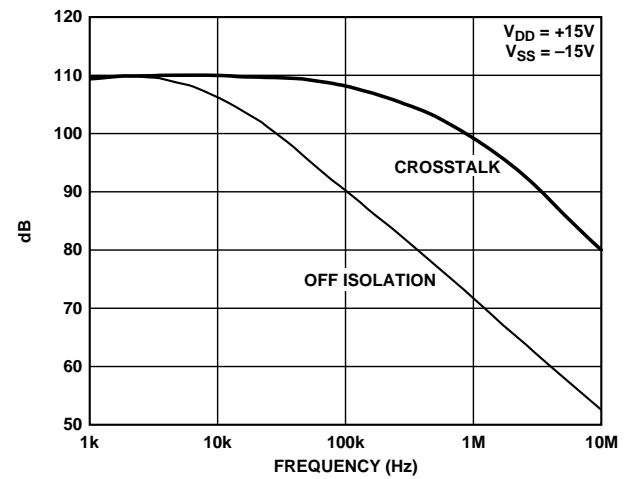
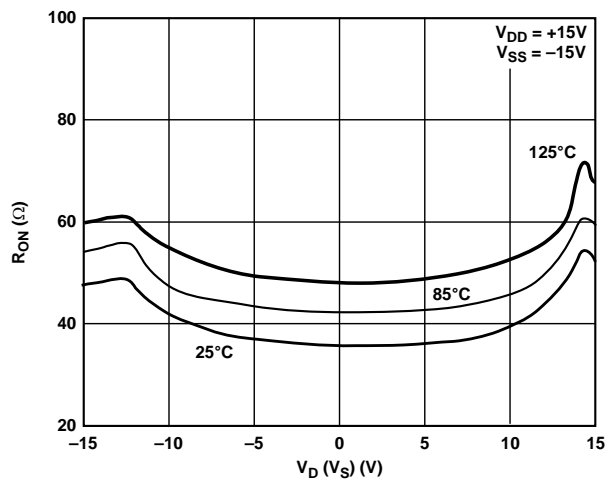
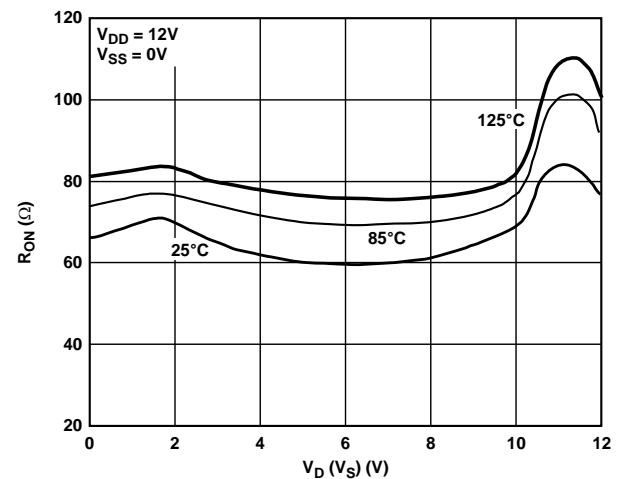
Figure 4.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ): Dual SupplyFigure 7. Leakage Currents as a Function of  $V_S$  ( $V_D$ )Figure 5.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ): Single Supply

Figure 8. Crosstalk and Off Isolation vs. Frequency

Figure 6.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ) for Different TemperaturesFigure 9.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures

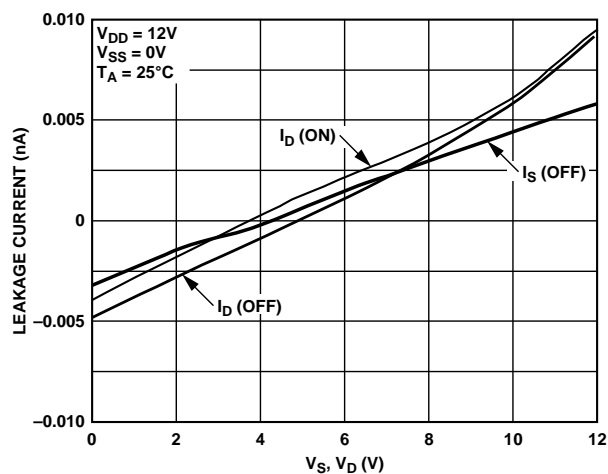


Figure 10. Leakage Currents as a Function of  $V_S$  ( $V_D$ )

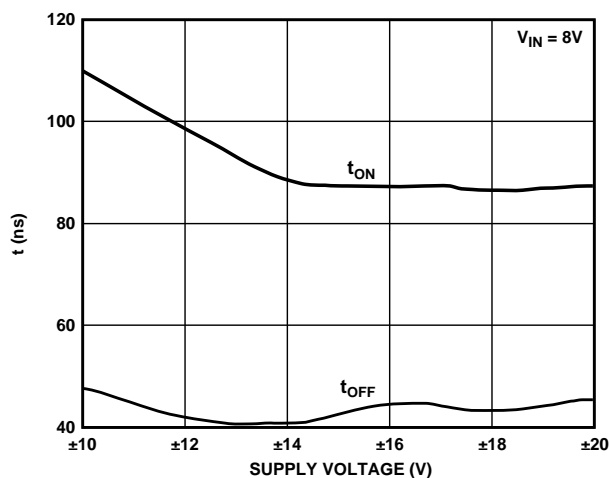


Figure 12. Switching Time vs. Bipolar Supply

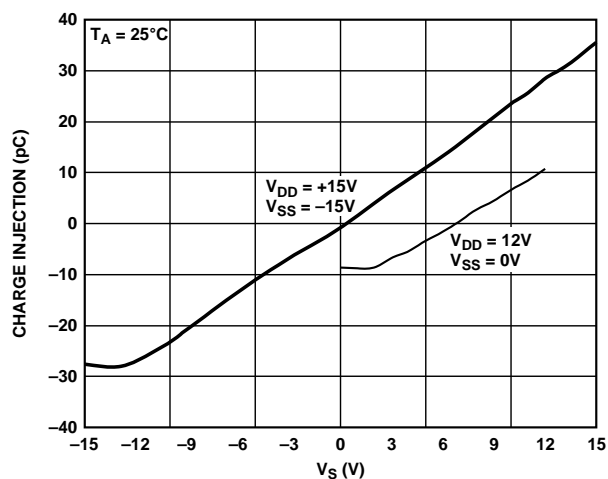


Figure 11. Charge Injection vs. Source Voltage

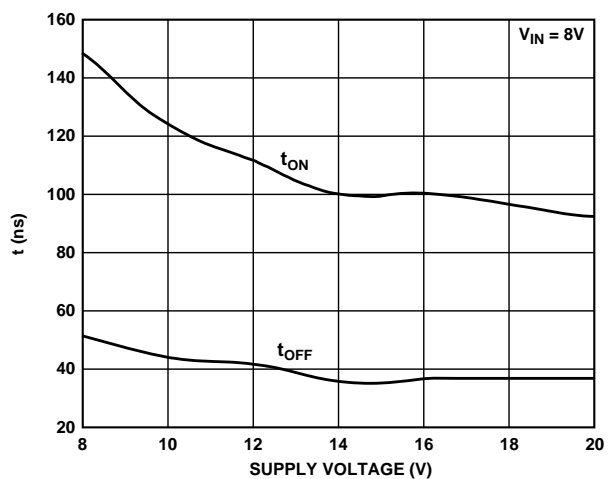


Figure 13. Switching Time vs. Single Supply



## TEST CIRCUITS

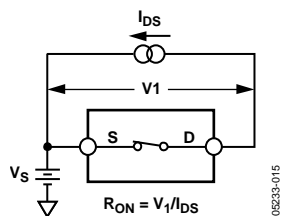


Figure 14. On Resistance

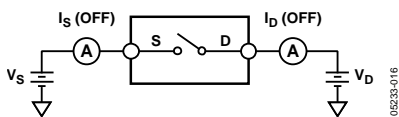


Figure 15. Off Leakage

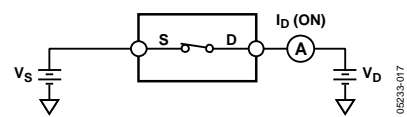


Figure 16. On Leakage

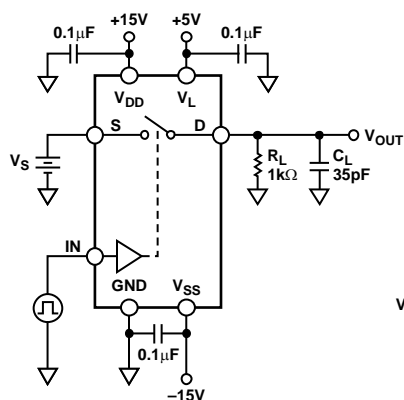


Figure 17. Switching Times

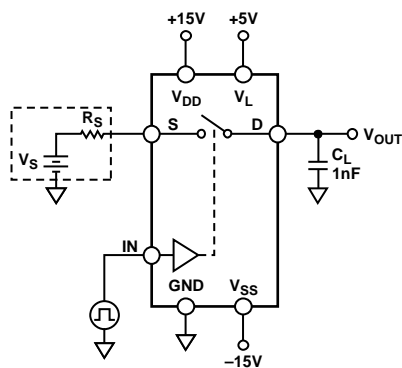
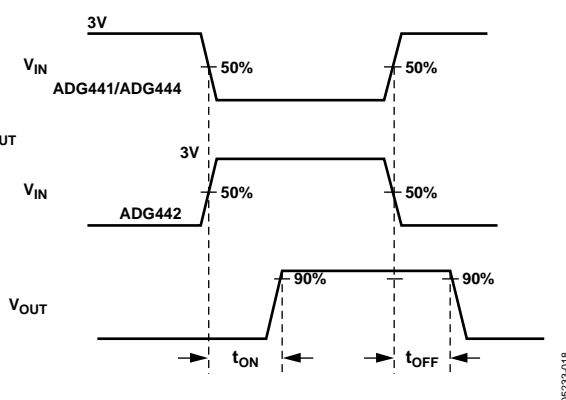
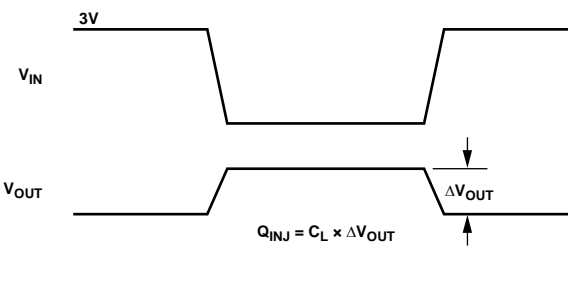
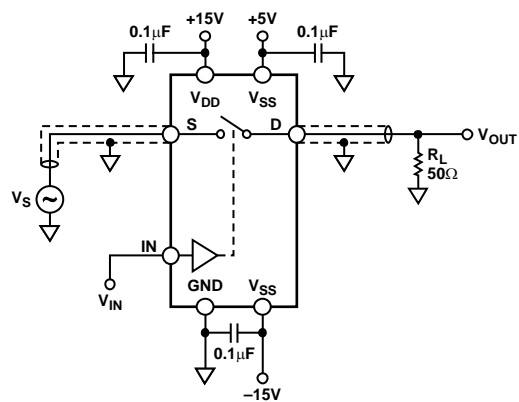


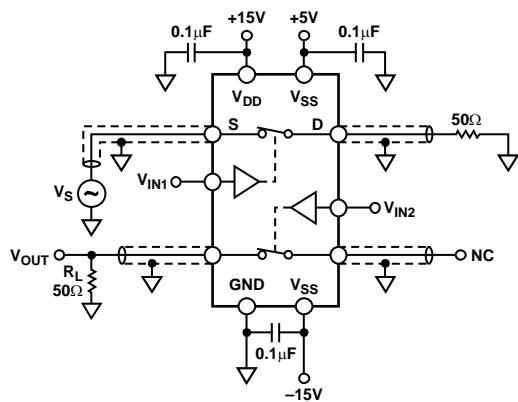
Figure 18. Charge Injection





05233-021

Figure 19. Off Isolation



05233-022

$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \times \text{LOG} |V_S/V_{OUT}|$$

Figure 20. Channel-to-Channel Crosstalk

## TERMINOLOGY

**R<sub>ON</sub>**

Ohmic resistance between D and S.

**R<sub>ON</sub> Match**

Difference between the R<sub>ON</sub> of any two channels.

**I<sub>S</sub> (OFF)**

Source leakage current with the switch OFF.

**I<sub>D</sub> (OFF)**

Drain leakage current with the switch OFF.

**I<sub>D</sub>, I<sub>S</sub> (ON)**

Channel leakage current with the switch ON.

**V<sub>D</sub> (V<sub>S</sub>)**

Analog voltage on Terminals D, S.

**C<sub>S</sub> (OFF)**

OFF switch source capacitance.

**C<sub>D</sub> (OFF)**

OFF switch drain capacitance.

**C<sub>D</sub>, C<sub>S</sub> (ON)**

ON switch capacitance.

**t<sub>ON</sub>**

Delay between applying the digital control input and the output switching on.

**t<sub>OFF</sub>**

Delay between applying the digital control input and the output switching off.

**t<sub>OPEN</sub>**

Break-before-make delay when switches are configured as a multiplexer.

**Crosstalk**

A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.

**Off Isolation**

A measure of unwanted signal coupling through an OFF switch.

**Charge Injection**

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

## TRENCH ISOLATION

In the [ADG441A](#), [ADG442A](#), and [ADG444A](#), an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode becomes forward-biased. A silicon-controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current which, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up proof switch.

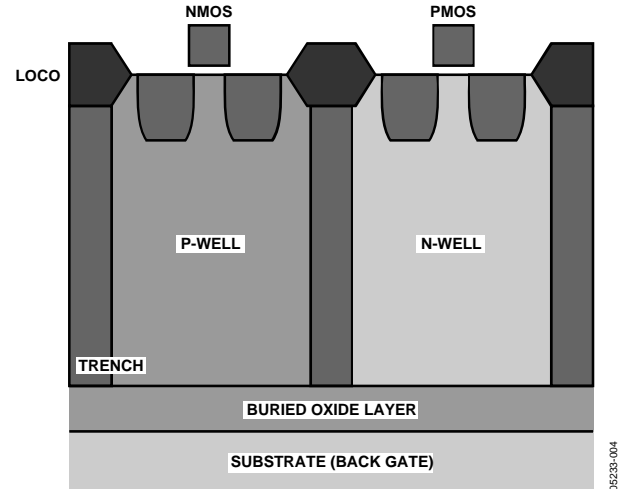
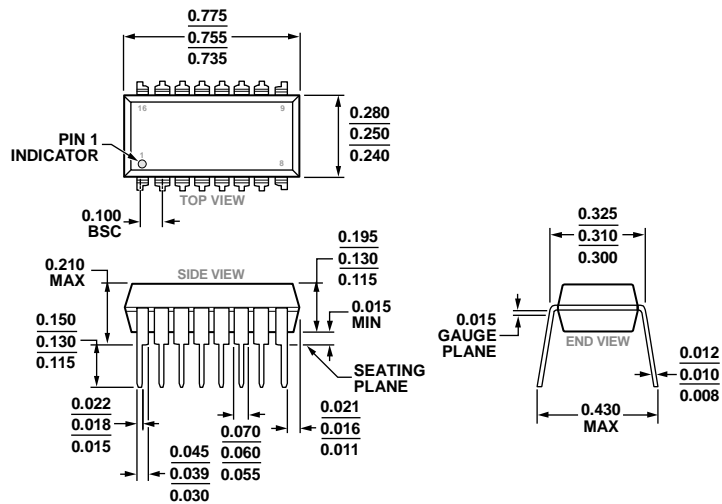


Figure 21. Trench Isolation

## OUTLINE DIMENSIONS

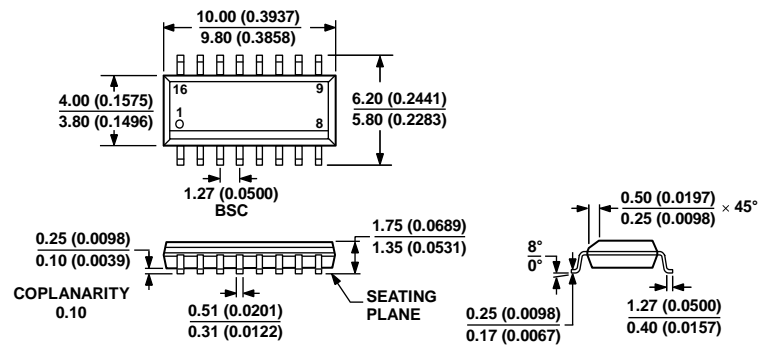


COMPLIANT TO JEDEC STANDARDS MS-001-BB

Figure 22. 16-Lead Plastic Dual In-Line Package [PDIP]  
Narrow Body  
(N-16)

Dimensions shown in inches

03-07-2014-D



COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 23. 16-Lead Standard Small Outline Package [SOIC\_N]  
(R-16)

Dimensions shown in millimeters and (inches)

060606-A

## ORDERING GUIDE

Model <sup>1,2</sup>	Temperature Range	Package Description	Package Option
ADG441BNZ	–40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG441BR	–40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG441BR-REEL	–40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG441BRZ	–40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG441BRZ-REEL	–40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG441ABCHIPS		DIE	
ADG441ABR-REEL	–40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG441ABRZ-REEL	–40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG442BNZ	–40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG442BRZ	–40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG442BRZ-REEL	–40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG444BNZ	–40°C to +85°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
ADG444BR	–40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG444BR-REEL	–40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG444BRZ	–40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16
ADG444BRZ-REEL	–40°C to +85°C	16-Lead Standard Small Outline Package [SOIC_N]	R-16

<sup>1</sup> Z = RoHS Compliant Part.<sup>2</sup> A = Trench isolated.

## NOTES

**NOTES**